

## METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

### ABSTRACT

An improved method of making CMOS surface channel transistors using fewer masking steps. In-situ doped poly silicon deposition can be used to reduce problems with poly depletion effects in transistor gates. In addition, using this method, the number of layers in each gate dielectric, the dielectric type, and dielectric thickness between n-  
5 channel and p-channel devices can be separately controlled. This method also allows the use of a lithography mask normally used to fabricate buried channel devices for use in fabricating surface channel devices, thus saving the manufacture of an additional mask.

"Express Mail" mailing label number: EL671638591US

Date of Deposit: March 14, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.